

<b>Notice of References Cited</b>	Application/Control No. 10/066,539	Applicant(s)/Patent Under Reexamination LIEN ET AL.	
	Examiner John J. Tabone, Jr.	Art Unit 2138	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Das et al., A low cost approach for detecting, locating, and avoiding interconnect faults in FPGA-based reconfigurable systems, Jan. 1999, Digital Object Identifier 10.1109/ICVD.1999.745159, Page(s):266 - 270.
	V	
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.